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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 09/802,021

Filing Date: March 08, 2001

Appellant(s): MEHRA ET AL.

Mark Kachigian
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 7, 2010 appealing from the Office action mailed December 9, 2009.

(1) Real Party in Interest

The examiner has no comment on the statement, or lack of statement, identifying by name the real party in interest in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The following is a list of claims that are rejected and pending in the application:
Claims 4,5,6,7,8,9,10,11,13,14,15,17 and 18.

(4) Status of Amendments After Final

The examiner has no comment on the appellant's statement of the status of amendments after final rejection contained in the brief.

(5) Summary of Claimed Subject Matter

The examiner has no comment on the summary of claimed subject matter contained in the brief.

(6) Grounds of Rejection to be Reviewed on Appeal

The examiner has no comment on the appellant's statement of the grounds of rejection to be reviewed on appeal. Every ground of rejection set forth in the Office action from which the appeal is taken (as modified by any advisory actions) is being

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maintained by the examiner except for the grounds of rejection (if any) listed under the subheading "WITHDRAWN REJECTIONS." New grounds of rejection (if any) are provided under the subheading "NEW GROUNDS OF REJECTION."

(7) Claims Appendix

The examiner has no comment on the copy of the appealed claims contained in the Appendix to the appellant's brief.

(8) Evidence Relied Upon

59995155	Schindler	11-1999
2006/0292292	Brightman	12-2006
6237079	Stoney	05-2001

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 4, 5, 6, 7, 8, 9, 10, 11, 13-15, 17, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al (US 5,995,155) in view of Brightman et al (US 2006/0292292) in view Stoney (US 6,237,079).

[claim 18]

In regard to Claim 18, Schindler et al discloses a receiver for digital data broadcast from a remote location (Figure 1 shows a satellite 112 and the antenna connected to the personal computer 118 therein, a receiver 316 is included in the personal computer 118 shown in Figure 3 as further described in column 7 line 46-64 and column 10 line 15-24);, said receiver comprising:

- A storage means for selective storage of digital data broadcast from a remote location (Figure 3 shows a storage system includes a tape drive 330, a disk drive 332, a CD ROM drive 334, a diskette drive 336, and a RAM 314 wherein different storages are selected to store different information as further described in column 9 line 47-line and column 10);
- A control system for control of the storage means and control of storage of data therein, the control system including a "first in first out" buffer being capable of receiving instructions in generic form (A control system includes a handheld remote 124, keyboard 126, a RF receiver 324 and a processor 310. Figure 9A and figure 10 show the handheld remote 124 and keyboard 126, which are further described in column 9 line 12-14; Figure 3 shows the RF receiver 324 and processor 310 as further described in column 9 line 26-46. Furthermore, the first

in first out "FIFO" buffer receives generic instructions on user and system

functions as described in Column 11 Lines 10-67); however, fails to disclose

- The data to be stored including instruction data, block data, and paths for the data being decoupled;
- a control processing unit for analyzing the digital data to determine when it should be stored
- And control processing unit inserting instructions in generic form into the single storage-instruction "first in first out" buffer said instructions comprising:
 - Register read and write commands in a generic form for the control of storage of digital data in the storage means
 - Control system commands for automating the bulk transfer of digital data to and from storage means
 - Wherein the single storage-instruction first in and first out buffer the control commands for automating the bulk transfer of the digital data from the control system are compatible and intermixable with register read and write commands

Brightman et al discloses a digital processing apparatus for communication of data and further comprising:

- A control processing unit for analyzing the digital data to determine when it should be stored (Figure 40 shows the processing of instructions to the FIFO)

- And control processing unit inserting instruction into the single "first in and first out" buffer (Figure 40 shows the instructions being processed via the FIFO for reading and writing commands) said instructions comprising:
 - Register read and write commands for the control of storage of digital data in the storage means (Paragraphs 0484-0486 describes the read and write commands for controlling of storage of digital data);
 - Control system commands for automating the bulk transfer of digital data to and from storage means (Paragraphs 0486 describes the control system commands transferring large amounts of data to the storage means);
 - Wherein the single first in and first out buffer the control commands for the control system are compatible and intermixable with register read and write commands (Paragraphs 0480-0490 describes the commands that are compatible with throughout the system).

Brightman et al teaches a system for processing and transferring of data through the use of FIFO and commands. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the system of receiving data from a remote location, as disclosed by Schindler et al, and further incorporate a system that provides read and write commands, as disclosed by Brightman, to allow for proper control of control commands and efficient storage of data.

Stoney teaches a system for controlling computing system comprising a FIFO wherein

- The data to be stored including instruction data, block data, and paths for the data being decoupled (Column 44 Lines 20-57 describes the data being stored on the system to contain instruction data. Furthermore, Column 54 Lines 21-67 describes the block data also being present in the storage device. The system provides separate paths for the data being processed and stored as described in Column 10 Lines 44-67);
- Using a single storage instruction "first in first out buffer" (Column 115 Lines 1-15 describes the ability to use a single FIFO buffer for the processing) said instructions including read and write commands in a generic form for the control of storage of the digital data (Column 25 Lines 40-67 describes the registering of read and write commands).

It is taught by Stoney to provide a system for processing and storing data on a single FIFO in order to provide higher performance memory solutions. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to use the system of receiving data from a remote location, as disclosed by Schindler et al in view of Brightman, and further incorporate a system that uses various data being stored on a single FIFO, as disclosed by Stoney, to allow for efficient storage of data.

[Claim 4]

In regard to Claim 4, Schindler et al discloses a system contains a receiver and a CPU as shown in Figure 3 and described in column 9 line 33-36; however, fails to disclose the receiver which characterized in that the analysis, storage and directing of the

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incoming data into the receiver is performed by a control processing unit (CPU) in the receiver. Stoney et al teaches that the analysis, storage, and directing incoming data into the system is performed by the CPU as seen in figure 1 and described in column 10 Lines 40-67. Thereby the analysis and storage of incoming data can be done quickly. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system, disclosed by Schindler, and incorporate the receiver with analysis, storage, and directing of incoming data, as disclosed by Stoney, providing the same motivation as described in Claim 18.

[Claim 5]

In regard to claim 5, Schindler et al discloses a system contains a receiver that can control which data to be stored; however, fails to disclose that the receiver in the system can control which data can be stored. Stoney et al teaches controlling of storage of data through the read and write commands (Column 25 Lines 40-67). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the system, disclosed by Schindler, and incorporate the receiver with analysis, storage, and directing of incoming data, as disclosed by Stoney et al, providing the same motivation as described in Claim 18.

[Claim 6]

In regard to claim 6, Schindler et al discloses a system contains a receiver, a CPU, and FIFO buffer. The FIFO buffer can include data which is altered by the CPU as described in Column 10, lines 43-49 and Column 11, lines 9-11; however, fails to disclose that the CPU can load the command signals data into the FIFO. Brightman et

al teaches controlling of storage of data through the read and write commands (paragraphs 0484-0486).

[Claim 7]

In regard to claim 7, Schindler et al discloses a system contains a receiver and a CPU wherein the command signal instructs the transfer of data to and/or from the data storage means as described in Column 22, line 43-line48; however, fails to disclose the command can also be generated from the CPU. Brightman et al teaches controlling of storage of data through the read and write commands via the CPU (paragraphs 0484-0486).

[Claim 8]

In regards to claim 8, Schindler et al discloses a system that contains a receiver wherein the command signal alter the start time for the storage of portions of incoming data as described in Column 21, line 46-57 and Column 22, line 1-9; however, Schindler et al fails to use a FIFO buffer to hold the command. Brightman et al teaches controlling of storage of data through the read and write commands wherein the commands are held in the FIFO based on the CPU commands (paragraphs 0484-0486).

[Claim 9]

In regard to claim 9, Schindler et al discloses a system contains a receiver, FIFO buffer and attached storage means shown in figure 3 and described in column 22 line 10-15; however, fails to disclose instruction in the FIFO in a generic form allows any possible register read/write command to be sent from/to the attached storage means.

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Brightman et al teaches controlling of storage of data through the read and write commands (paragraphs 0484-0486).

[Claim 10]

In regard to claim 10, Schindler et al discloses a receiver and attached storage means as shown in figure 3. Furthermore, the storage means is an ATA or ATAPI compatible device as seen in figure 3 which shows a CD ROM drive 334 (ATA stands for Advanced Technology Attachment, compatible device including Compact Disk Read Only Memory, which is CD ROM); however, Schindler et al fails to include the ATA compatible inside the receiver. It is well known in the art that the ATA or ATAPI compatible device can be place inside a receiver as storage. It would increase the storage capacity infinitely when use CD ROM for the memory storage system inside a receiver. Furthermore, when one CD is full, it can be replaced with a new CD so that the recording section can continue without losing a lot of information. Therefore, the examiner takes official notice that it would be obvious to use an ATA or ATAPI compatible device inside a receiver for recording purpose.

[Claim 11]

In regard to claim 11, Schindler et al discloses a receiver and a HDD as shown in figure 3. Schindler et al also discloses that bulk transfer of the streamed data to the storage means as described in column 3 lines 51-67 and column 4 lines 1-11; however, fails to address any addition information, which is not used to provide the register read/write command to the HDD. Brightman et al teaches controlling of storage of data through the read and write commands (paragraphs 0484-0486).

[claim 13]

In regard to Claim 13, Schindler discloses a receiver wherein said command signals in the first in first out buffer allows a combined set of command signals to be generated (Column 19, line 1-10 describes the combined command signals of the FIFO).

[claim 14]

In regard to Claim 14, Schindler discloses a receiver wherein the storage means is an advanced technology attachment pack interface compatible device (Figure 1 shows the system wherein it is well known in the art that the devices have an interface compatible device).

[claim 15]

In regard to Claim 15, Schindler discloses a receiver that is connected to a storage means that allows selective storage of received data (Figure 1 shows a receiver that is connected to a storage device CPU for selective storage of received data).

[claim 17]

In regard to Claim 17, Schindler et al discloses a receiver wherein the data required during said bulk transfer is a multiplex of many data streams (Figure 1 shows a satellite 112 and the antenna connected to the personal computer 118 therein, a receiver 316 is included in the personal computer 118 shown in Figure 3 as further described in column 7 line 46-64 and column 10 line 15-24).

(10) Response to Argument

Appellant's arguments filed June 7, 2010 have been fully considered. Regarding the applied references of Schindler et al (US 5,995,155) in view of Brightman et al (US 2006/0292292) in view Stoney (US 6,237,079) failing to disclose, teach or suggest "a "first in first out" buffer being capable of receiving instructions in generic form" as recited in independent Claim 18. It is noted Schindler et al discloses in Column 11 Lines 10-67 the FIFO buffer receives information that is written onto the buffer. The information written to the buffer is both MPEG data that has been buffered as well as control commands provided from the user and the system. This type of information provides a "generic form" of information being placed into the buffer. The examiner notes that the claim limitation "generic form" is being used as defined by the American Heritage College dictionary which defines generic as "relating to or descriptive of an entire group or class". Therefore the information as disclosed by Schindler is generic form of group information pertaining to command information and MPEG information. It is important to note that information stored on the FIFO is in generic form prior to be processed by the system as described in Column 11 Lines 5-67. Additionally, appellant argues on pages 10 –he prior art of record fails to disclose, suggest, or teach "control processing unit inserting instructions in generic form into the "first in first out buffer" as recited in independent Claim 18. It is noted as stated above Schindler et al discloses the ability of inserting instructions/commands into the FIFO as described in Column 11 Lines 10-67; however, is silent regarding the commands be read/write commands. Therefore, Brightman et al is being used to teach the ability to intermix read/write commands on the buffer as described in paragraphs 0484-0486. Therefore, the above applied

references show the storing and intermixing of generic forms that are being stored on the FIFO buffer.

In response to appellant's argument that there is no teaching, suggestion, or motivation to combine the references, the examiner recognizes that obviousness may be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), and *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007). In this case, Brightman is used to further teach the processing and transferring of data through FIFO commands and in particular read/write commands which is silent in Schindler et al. Additionally, Stoney is used to provide a more effective and higher performance memory solution to a single FIFO that is silent in the two previous references. Each reference provides improvements to the system for transferring and storing data into the FIFO in a more efficient manner.

Furthermore, on page 12 appellants argues the combination of references in reference to SKR guidelines. It is noted that the combination of the familiar elements with the applied prior art provides known methods in the art that does not yield a predictable result and therefore the elements used in combination do more together in the applied system they would in a separate sequential operation. In this present application the base reference Schindler teaches the storing of data in the FIFO to

generic commands; however, is silent regarding the registering of read and write commands for controlling the system as well as bulk transfer of the registered commands. Brightman clearly teaches the registering of read and write commands to the FIFO and thereby is applied in order to further provide this type of registering of commands to make a more effective processing of commands within the system. Furthermore, Stoney is used to teach the decoupling of the data stored including instruction data, block data, and paths for the data being decoupled. The features as further taught by Stoney allow for instructions to be properly stored on the FIFO and thereby allows for a higher performance memory solutions to the system. Thereby it can be seen the use of these three references in combination allows for a more effective memory solutions to the system.

Additionally, appellant argues on page 13 that the examiner never identifies the level of skill or background of a person ordinary skilled in the art. Through an enablement determination based on the specification of the current application a person of ordinary skill in the art would need a college level or master level degree. A person of ordinary skill in the art based on the nature of the invention, the state of the prior art, the relative skill of those in the art, the predictability of the art and the breath of the claims (*In re Wands*, 858F2d 731 (Fed. Cir. 1988)) would require a technical background to properly fill in the technical gaps left by the specification as well as the full scope of claims. Furthermore, appellant repeatedly mentions the lengthy prosecution and new references being applied; however, the examiner notes further

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search and reconsideration is taken each time the claims are amended and newly applied references are found in order to provide a high quality level of prosecution.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

/JAMIE JO ATALA/

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